

Application No.: 09/466,180
Amendment dated: June 2, 2005
Reply to Office Action dated: December 3, 2004

REMARKS

Claims 1, 3-4, 6-12, and 14-30 are pending in the application. Claims 2, 5, and 13 have been cancelled. No claims have been amended.

Claims 1, 3-4, 6-12, and 14-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins et al, U.S. Patent No. 5,937,436 (hereinafter "Watkins") in view of Horstmann et al, U.S. Patent No. 6,125,433 (hereinafter "Horstmann"), further in view of Futral et al, U.S. Patent No. 5,991,797 (hereinafter "Futral") and further in view of Garcia et al., U.S. Patent No. 6,163,834 (hereinafter "Garcia").

Applicants respectfully submit that the cited references do not teach, suggest or disclose "[a] host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising: ... to store selected translation and protection table (TPT) entries from said host memory for a data transaction, *each TPT entry comprising protection attributes to control read and write access to a given memory region of said host memory, ... and a memory protection tag to specify whether said host-fabric adapter has permission to access said host memory; wherein said host-fabric adapter is configured to flush individual cached TPT entries from said internal cache in accordance with the corresponding translation cacheable flag*".

The Office Action cites column 4, lines 35-50 of Watkins as disclosing protection attributes to control read and write access to a given memory region of said memory. The cited section states:

A sample physical translation format 281 is also shown in FIG. 2B. In one embodiment, this format 281 includes a valid bit 283, protection bits 285 and the actual physical page bits 287. The valid bit 283, in the descriptor, determines if a specific translation entry will be placed into the ATU (if valid bit 283 is set) or ignored (if valid bit 283 is cleared). *The protection bits 285 are transferred through control line 560 of FIG. 5 in determining whether a page is accessible using the ATU's physical translation for the virtual address.* For instance, a read-only page can be protected from writes with a read only page protection bit.

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The physical page bits 287 provide the virtual to physical address mapping for the corresponding portion of the data buffer in virtual address space. The data buffer pointed to by the data buffer pointer 273 can span one or more virtual pages and are not necessarily contiguously placed in physical memory (*emphasis supplied*).

Applicants submit that the cited sections do not teach "...protection attributes to control read and write access to a given memory region of said host memory..." as disclosed in the embodiment of claim 1. The protection bits disclosed in Watkins are directed towards the Watkins ATU or a physical translation unit (see above), *not* towards a memory unit. The Watkins ATU or address translation unit ("ATU"), is described as follows: "an "address translation" is mapping between a virtual address and physical address" (column 1, lines 23-25). Therefore, the protection bits of Watkins are not addressed "...to control read and write access to a given memory region..." as disclosed in embodiments of Applicants' invention, but rather directed toward a temporary mapping feature of Watkins. The "protection bits" used in the context of a address translation unit as disclosed in Watkins are insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

Next, the Office Action states that Garcia teaches a memory protection tag to specify whether an adapter has permission to access said memory (e.g., fig. 6, tag protection check field, col. 2 lines 20-55). Applicants respectfully disagree and maintain that nowhere in the extensive section cited by the Office Action is the disclosure of a memory protection tag *to specify whether said host fabric adapter has permission to access* a host memory. The reference merely discloses a "protection tag" and states that it is stored in the context memory during the virtual interface creation process. The "protection tag[s]" disclosed in Garcia are again insufficient to form the basis of a proper 35 U.S.C. §103(a) rejection of independent claim 1.

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Futral '797 and Horstmann fail to make up for the deficiencies of Garcia and Watkins.

Therefore, none of these features are found in the Watkins, Garcia, Futral '797 or Horstmann references taken individually or in combination. Since features of each of the pending claims are not taught or suggested by the cited references, reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

Conclusion

For at least all the above reasons, the Applicants respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

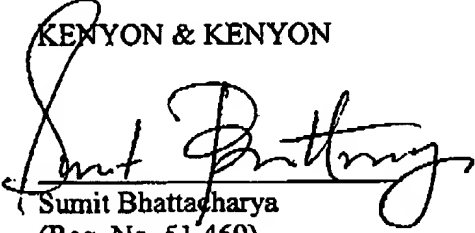
The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

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